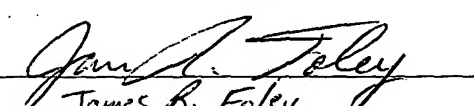


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James R. Foley

Attorney Docket No. 1488/40499 Case No. 02-4828

### High-k dielectric gate material uniquely formed

Inventors: Sheldon Aronowitz, Vladimir Zubkov, and Grace Sun

#### BACKGROUND

Silicon dioxide ("SiO<sub>2</sub>") has dominated semiconductor technology as the universal  
5 dielectric for gate material. As the overall geometry of devices has shrunk over the years, the  
thickness of the silicon dioxide dielectric gate also has had to be decreased. As the silicon  
dioxide gate thickness decreases, problems arise, such as boron penetration in p-channel devices  
and tunnel leakage from the silicon substrate to the polysilicon gate ultimately culminating in  
direct band-to-band tunneling. There is therefore a need for replacement by a suitable high-k  
10 dielectric material.

Search for suitable high-k dielectric materials has focused primarily on hafnium oxide,  
zirconium oxide, and related compounds. These materials present difficulties in use as a gate  
material, including the occurrence and control of microcrystallization, migration of zirconium to  
the silicon interface, and boron penetration for p-channel devices. Because these oxides cannot  
15 be exactly matched to the silicon surface, the density of interface states associated with these and  
similar materials remains about one to two orders of magnitude higher than for gates made of

silicon dioxide, even when applied by atomic layer deposition, the most controllable deposition process.

Accordingly, a need exists for a relatively high-k (greater than 10) dielectric gate material  
20 that avoids these difficulties, reduces the chances of electrons being trapped in the dielectric, and  
minimizes penetration effects, yet allows for the very small equivalent oxide thicknesses  
required for ever smaller devices.

#### SUMMARY

A new relatively high-k gate dielectric gate material is identified. Calcium oxide is  
25 deposited on the silicon wafer by atomic layer deposition. It can be made sufficiently thick so as  
to reduce current leakage from the silicon substrate to the polysilicon gate, prevent boron  
penetration in p-channel devices, and reduce electron trapping in the dielectric. Calcium oxide's  
lack of effective electron affinity reduces electron trapping. Additionally, the calcium oxide  
structure provides a high barrier to boron penetration in a p-channel device.

#### 30 BRIEF DESCRIPTION OF THE DRAWINGS:

Figure 1 is a depiction of the use of calcium oxide as a dielectric gate material on a silicon wafer.

Figure 2 is a block diagram of one embodiment of the method of the present invention.

Figure 3 is a block diagram of another embodiment of the method of the present invention.

#### DESCRIPTION OF THE INVENTION

35 The organization and manner of the structure and operation of the preferred embodiments  
of the invention, together with further objects and advantages thereof, may best be understood by  
reference to the following description, taken in connection with the accompanying drawings.

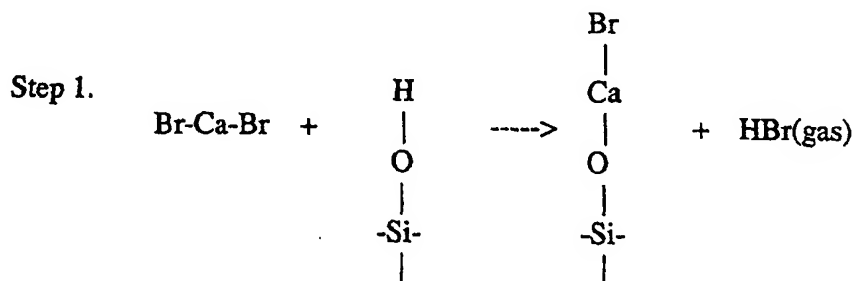
The application of calcium oxide to the silicon wafer is accomplished by high-  
temperature atomic layer deposition. The use of calcium oxide is depicted in Figure 1. The

40 method of application is depicted in block diagram form in Figure 2. The surface of a silicon wafer is prepared such that it is saturated with respect to hydroxyl groups (-OH) completing any dangling silicon bonds. The preparation methods are known to those skilled in the art.

In a suitable reactor, a calcium halide, preferably calcium bromide, is heated to a temperature such that its vapor pressure is sufficiently large that deposition can be achieved at a  
 45 reasonable rate. For example, at 825 °C, the vapor pressure of CaBr<sub>2</sub> equals approximately 5 mTorr. Under these conditions, a fully hydroxylated eight-inch silicon wafer can be completely covered in five minutes if the flow rate is 1000 sccm.

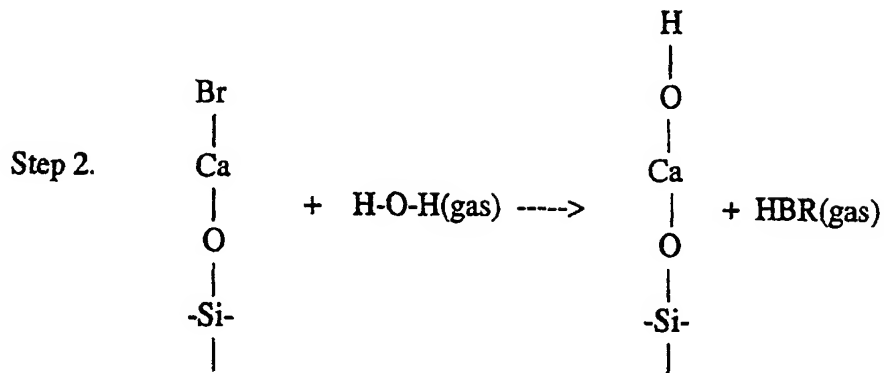
A nonreactive carrier gas, such as neon or argon, heated to the temperature of the calcium halide, transports the calcium halide to the wafer in the first step of this process. The wafer  
 50 surface will be heated by the carrier gas to a sufficiently high temperature to promote a condensation reaction between the hydroxyl groups and the calcium halide. The temperature maintained at the wafer surface is such that any excess calcium halide that has not reacted with a hydroxyl group simply sublims, that is, it cannot remain at the surface, thereby ensuring that a monolayer is formed. This first step is illustrated below using calcium bromide (CaBr<sub>2</sub>):

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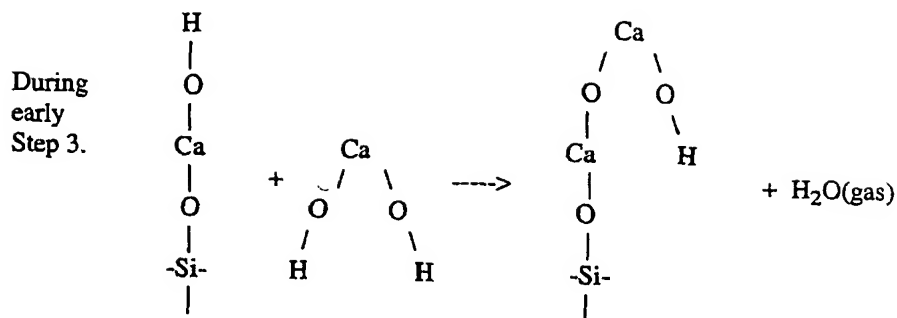
The Ca-O bond, shown above, is a very strong bond, about 4.6 eV.

Gaseous water is next transported by the heated carrier gas, to hydroxylate the calcium and release HBR (gas) in the second step:



The third step is the ultimate deposition of calcium oxide by first transporting calcium (gas) at a controlled flow rate to create a monolayer of calcium on the wafer. This transport is followed by transporting water (gas) to the wafer. The hydroxylation reaction,  $\text{Ca} + 2\text{H}_2\text{O} \rightarrow \text{Ca(OH)}_2 + \text{H}_2$ , occurs even at room temperature. The wafer is heated to temperatures in the range of 600 °C to 800 °C in order to overcome possible kinetic barriers to the reaction shown in Step 3.

The sequential process (depositing calcium followed by exposure to gaseous water and heat) is repeated until the desired thickness of dielectric is obtained. At every thermal step a bimolecular condensation occurs such as displayed in Step 3. Shown schematically is an early stage in the third-step deposition process:



The procedure also is presented schematically in Figure 2. The result is an amorphous layer of calcium oxide, grown to the thickness required by the application for which the material will be used.

The first two steps in this process are atomic layer deposition; they are self-limiting. Step 3 represents atomic layer epitaxy; it is less restrictive but not self-limiting.

An alternative procedure that would be a self-limiting atomic layer deposition process utilizes the reactions in steps 1 and 2. Here a calcium halide in the vapor state, preferably  $\text{CaBr}_2$ , is transported to the surface after step 2. The surface is heated to a sufficiently high temperature that the condensation process depicted in step 1 occurs. Unreacted  $\text{CaBr}_2$  is vaporized in this procedure. Gaseous water, transported by a heated carrier gas, then is introduced. As shown in Step 2, the gaseous water will hydroxylate the calcium and release  $\text{HBr}$ . The process is continued until a desired deposition thickness is achieved. This alternative procedure is shown in Figure 3.

Since, as calculations show, calcium oxide does not display any effective electron affinity, if the density of structural defects is low, trapping of electrons will be markedly reduced. Accordingly, this feature of no electron affinity, which is also calculated for an ideal  $\text{SiO}_2$ , is a desirable one for a gate dielectric.

Boron penetration from a heavily doped  $p^+$  polysilicon gate at temperatures currently

used for annealing is a problem. Calculations show that calcium oxide exhibits a very high barrier (approximately 4 eV) to such penetration and subsequent diffusion. This feature is particularly attractive for a gate dielectric. Therefore, calcium oxide formed in this unique  
90 manner will act as an effective, high-k dielectric gate material.

While preferred embodiments of the present invention are shown and described, it is envisioned that those skilled in the art may devise various modifications of the present invention without departing from the spirit and scope of the appended claims.